Claims

Claim 1. (Currently Amended) A device for analyzing digital data formulated in accordance with a communication protocol, comprising:

a. a data memory for storing the digital data to be analyzed;

b. a microcode memory for storing a microcode that represents at least part of the communication protocol;

c. a data register for reading out a pre-determined number of bits from the data memory;

d. a microcode register for reading out a pre-determined number of bits from the microcode memory, with the content of the microcode register being usable for analyzing the content of the data register;

e. an output memory into which the results of the analysis are entered;

f. a first addressing unit for addressing the data memory; and

g. a second addressing unit for addressing the microcode memory, with the first and second addressing units being designed to take into account the content of the data register and/or the microcode register when ~~the corresponding~~ subsequent addresses are determined.

Claim 2. (Currently Amended) The device according to claim 1 wherein the first and second addressing units each comprise at least one counter that may be changed ~~when the addresses~~ in accordance with the content of the data register and/or microcode register when the subsequent addresses are determined.

Claim 3. (Currently Amended) The device according claim 1 wherein the data ~~range~~ register is designed to align and/or shift its content.

Claim 4. (Currently Amended) The device according to claims 1, 2 or 3 further comprising a register block with at least one register and at least one counter, the contents of which are taken into account for determining the ~~relevant~~ subsequent addresses ~~of the data register and/or the microcode register~~ for the first and second addressing units, the at least one register and the at least one counter being used to take into account the contents of the data register and/or the microcode register ~~of preceding points in time that are decisive for the addresses~~.

Claim 5. (Original) The device according to claim 4 further comprising a third addressing unit for the output memory, with the address of the third addressing unit being changeable by taking the content of the microcode register into account.

Claim 6. (Original) The device according to claim 5 further comprising a logic circuit with which an entry into the output memory is read out, changed to take into account a new result, and rewritten into the output memory.

Claim 7. (Original) The device according to claim 6 wherein a starting address is loaded into the addressing units.

Claim 8. (Original) The device according to claim 7 where the digital data to be analyzed are protocol data units that contain parameters, and the results entered into the output memory have at least one parameter identifier and at least one parameter value.

Claim 9. (Original) The device according to claim 8 wherein at least two of the memories are combined in one physical memory, and the corresponding addressing units are combined in one physical addressing unit.

Claim 10. (Original) A method of analyzing digital data formulated in accordance with a communication protocol comprising the steps of:

a. loading the digital data to be analyzed into a data memory;

b. loading a microcode into a microcode memory, with the microcode representing at least part of the communication protocol;

c. reading out a pre-determined number of bits from the data memory into a data register in accordance with an address specified by a first addressing unit;

d. reading out a pre-determined number of bits from the microcode memory into a microcode register in accordance with an address specified by a second addressing unit;

e. assigning functions to the data bits in the data register according to the microcode bits in the microcode register;

f. entering at least one result of the assignment in an output memory; and

g. updating counter readings for the first and second addressing units in accordance with the content of the data register and/or the microcode register.

Claim 11. (Currently Amended) The method according to claim 10 wherein the entry in accordance with step f) takes place at an address specified by a third addressing unit, with a counter reading for the third addressing unit being updated in accordance with the content of the ~~data register and/or~~ the microcode register.

Claim 12. (Original) The method according to claim 11 wherein prior to entry in accordance with step f) an incomplete entry is read out from the output memory by a logic circuit and changed to take into account a new result, and then rewritten into the output memory.

Claim 13. (Original) The method according to claims 10, 11 or 12 comprising in a further step a register block containing at least one register and at least one counter which is loaded with the results of the analysis and which are taken into account when ~~the corresponding~~ subsequent addresses ~~of the data register and/or the microcode register of subsequent points in time~~ are determined for the first and second addressing units.